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McDermott, Will & Emery
600, 13th Street, N.W.,
Washington, DC 20005-3096

EXAMINER	
ODOM, CURTIS B	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/812,694	NISHIMURA ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because in Figure 13, block 1301, "Binarization Circuit" is suggested to be changed to "Digitization Circuit". Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because the word "binarization" is suggested to be changed to "digitization". Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

a. On page 7, line 22, "Vth" is suggested to be changed to "threshold value".

b. On page 18, lines 18-21, the phrase "a first output value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive and the above-mentioned given reference value" is suggested to be changed to "a first output value and the above-mentioned reference value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive."

c. On page 8, line 24-page 9, line 6, the phrase "the first output value after the sign of the output of the above-mentioned adaptive equalizer circuit is changed from positive to negative and the first reference value, and the equalization characteristics are changed based on the first output value after the sign of the output of the above-mentioned adaptive equalizer circuit is changed from negative to positive and the second reference value" is suggested to be changed to "the first output value and the first reference value after the sign of the output of the above-mentioned adaptive equalizer circuit is changed from positive to negative, and the equalization characteristics are changed based on the first output value and the second reference

value after the sign of the output of the above-mentioned adaptive equalizer circuit is changed from negative to positive".

d. On page 9, lines 11-17, the phrase "the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative and the second reference value, and the equalization characteristics is changed based on the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from negative to positive and the first reference value" is suggested to be changed to the second reference value and the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative, and the equalization characteristics is changed based on the first reference value and output value immediately before the sign of the output of the adaptive equalizer circuit is changed from negative to positive".

e. On page 9, line 21-pg. 10, line 3, the phrase "the first output value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive and the first reference value, and the equalization characteristics are changed based on the output value immediately before the sign of the output of the above-mentioned adaptive equalizer circuit is changed from positive to negative or negative to positive and the second reference value" is suggested to be changed to "the first output value and the first reference value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive, and the equalization characteristics are changed based on the second reference value and the output value immediately before the sign of the output of the above-mentioned adaptive equalizer circuit is changed from positive to negative or negative to positive".

f. On page 11, line 1, the word "binarizing" is suggested to be changed to "digitizing".

g. On page 13, line 7, "1301" is suggested to be changed to "1302".

h. On page 16, line 19, the word "sing" is suggested to be changed to "sign".

i. On page 19, line 2, the word "sigh" is suggested to be changed to "sign".

j. On page 19, lines 10-18, "CS0" is suggested to be changed to "C0s", "CS1" is suggested to be changed to "C1s", and "CSn" is suggested to be changed to "CnS".

k. On page 21, lines 1-15, "binarization" is suggested to be changed to "digitization", and "binarizes" is suggested to be changed to "digitizes".

l. Throughout the specification, the phrase "in synchronous" is suggested to be changed to "in synchronization".

Appropriate correction is required.

Claim Objections

4. Claims 1-9 are objected to because of the following informalities:

a. In claims 1-9, the phrase "in synchronous" is suggested to be changed to "in synchronization".

b. In claim 1, the word "inputted" is suggested to be changed to "input".

c. In claim 1, the phrase "the adaptive equalizer circuit has a constitution to change the equalization characteristics in which the arithmetic operation..." is suggested to be changed

to "the adaptive equalizer circuit changes the equalization characteristics wherein the arithmetic operation...".

d. In claim 1, the phrase ""a first output value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive and said given reference value" is suggested to be changed to "a first output value and said given reference value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive."

e. In claim 2, the phrase "the constitution to change the equalization characteristics is a constitution in which" is suggested to be deleted.

f. In claim 2, the phrase "the first output value after the sign of the output of the adaptive equalizer circuit is changed from positive to negative and the first reference value, and the equalization characteristics are changed based on the first output value after the sign of the output of the adaptive equalizer circuit is changed from negative to positive and the second reference value" is suggested to be changed to "the first output value and the first reference value after the sign of the output of the adaptive equalizer circuit is changed from positive to negative, and the equalization characteristics are changed based on the first output value and the second reference value after the sign of the output of the adaptive equalizer circuit is changed from negative to positive".

g. In claim 3, the phrase "the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative and the second reference value, and the equalization characteristics is changed based on the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from negative to positive

and the first reference value" is suggested to be changed to the second reference value and the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative, and the equalization characteristics is changed based on the first reference value and output value immediately before the sign of the output of the adaptive equalizer circuit is changed from negative to positive".

h. In claim 4, the phrase "said constitution which changes the equalization characteristics is a constitution in which" is suggested to be deleted.

g. In claim 4, the phrase "the first output value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive and the first reference value, and the equalization characteristics are changed based on the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative or negative to positive and the second reference value" is suggested to be changed to "the first output value and the first reference value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive, and the equalization characteristics are changed based on the second reference value and the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative or negative to positive".

h. In claim 8, the word "binarizing" is suggested to be changed to "digitizing".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 3 and 4 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 3 and 4 recite the claim limitations 'the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative and the second reference value, and the equalization characteristics is changed based on the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from negative to positive and the first reference value" and "the first output value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive and the first reference value, and the equalization characteristics are changed based on the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative or negative to positive and the second reference value". However, after reviewing the specification (specifically, Fig. 12, pages 18-20), it is the understanding of the examiner that the equalization characteristics are always changed using an output value and a reference value **after** the sign of the output of the adaptive equalizer circuit is changed from positive to negative or

negative to positive. There is an operation (from which this claim may be referring to) described (Fig. 12, pages 18-20) where the equalization characteristics are changed using a **preceding (delayed)** output value immediately before the sign of a **present** output value from the equalizer is changed from positive to negative or negative to positive.

7. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 7 recites the limitation "the adaptive equalizer circuit is operated by sampling an input signal with a reference clock signal in synchronous with the input signal and computes an output value of the adaptive equalizer circuit which is in synchronous with a signal having a phase different from the reference clock signal by a ½ clock cycle by an interpolation". However, after reviewing the specification, there is no specific description or illustration as to how an interpolation method/apparatus is implemented into the sampling process of the current device. The sampling process is adjusted using a PLL and delay device, but there is no specific description as to how interpolation is implemented into this process.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 2, 5, 6, and 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Kuribayashi (U. S. Patent No. 5, 768, 313) in view of Jonsson et al. (U. S. Patent No. 6, 414, 990)

Regarding claim 1, Kuribayashi discloses an adaptive equalizer circuit (Figs. 5, 7, 9, and 10, column 4, line 8-column 6, line 63) which adds given equalization characteristics to signals input through a transmission path and performs a control such that an equalization error (column 4, line 47-column 5, line 30) obtained by performing an arithmetic operation based on an obtained output (output from equalizer) and a given reference value (output from data discriminating circuit) is minimized thus obtaining equalization characteristics,

the improvement being characterized in that the equalization characteristics are changed (column 4, lines 16-column 5, line 30) by computing the equalization error based on a first output value after a sign of the output of the adaptive equalizer circuit is changed (output of zero crossing extractor) from positive to negative or from negative to positive and the given reference value (output from data discriminating circuit).

Kuribayashi does not disclose the arithmetic operation of the adaptive equalizer circuit is performed in synchronous with a signal having a phase different from the reference clock signal of the signal by a 1/2 clock cycle.

However, Jonsson discloses a timing circuit which allows the operation of an equalizer circuit to be performed in synchronous with a signal having a phase different from the reference clock signal of the signal by a delayed clock cycle by controlling the sampling operation of the circuit using a phase control signal (column 4, lines 51-65). Jonsson states that this phase control

signal can be a delayed signal which indicates a desired sampling time shift (column 4, lines 51-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the circuit of Kuribayashi with the teachings of Jonsson and have the operation of the adaptive equalizer circuit performed in synchronous with a signal having a phase different from the reference clock signal of the signal by a ½ delayed clock cycle to slow down the sampling phase to ensure accurate adjustment of the filter coefficients by avoiding updating the filter coefficients too fast. Jonsson states the sampling phase may shift without corresponding modification to the filter coefficients since if the sampling phase is too fast (column 4, lines 51-65).

Regarding claim 2, which inherits the limitations of claim 1, Kuribayashi discloses the equalization characteristics of the adaptive equalizer circuit are changed based on the first output value after the sign of the output of the adaptive equalizer circuit is changed from positive to negative (column 4, lines 17-46) and a first reference value (column 4, line 47-column 5, line 30, wherein the reference value is the value output from the data discriminator) and the equalization characteristics of the adaptive equalizer circuit are changed based on the first output value after the sign of the output of the adaptive equalizer circuit is changed from negative to positive (column 4, lines 17-46) and a second reference value (column 4, line 47-column 5, line 30, wherein the reference value is the value output from the data discriminator).

Regarding claim 5, which inherits the limitations of claim 2, Kuribayahsi discloses the second reference value is set to a value which inverts the sign of the first reference value (column 4, lines 47-67), wherein the first reference value is "-1", and the second reference value is "1".

Regarding claim 6, which inherits the limitations of claim 1, Kuribayashi discloses the equalization characteristics are changed based on the output value of the adaptive equalizer circuit (column 4, line 8-column 6, line 63). Kuribayashi does not disclose the adaptive equalizer circuit is operated to sample an input signal with a signal having a phase different from the reference clock signal which is in synchronization with the input signal by a 1/2 clock cycle.

However, Jonsson discloses a timing circuit which allows the operation of an equalizer circuit to be performed in synchronous with a signal having a phase different from the reference clock signal of the signal by a delayed clock cycle by controlling the sampling of the input signal using a phase control signal (column 4, lines 51-65). Jonsson states that this phase control signal can be a delayed signal which indicates a desired sampling time shift (column 4, lines 51-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the circuit of Kuribayashi with the teachings of Jonsson and have the operation sampling the input signal of the adaptive equalizer circuit performed in synchronous with a signal having a phase different from the reference clock signal of the signal by a ½ delayed clock cycle to slow down the sampling phase to ensure accurate adjustment of the filter coefficients by avoiding updating the filter coefficients too fast. Jonsson states the sampling phase may shift without corresponding modification to the filter coefficients since if the sampling phase is too fast (column 4, lines 51-65).

Regarding claim 9, which inherits the limitations of claim 1, Jonsson discloses the signals input to the adaptive equalizer circuit are signals optically read from a recording medium (column 3, lines 20-28).

Allowable Subject Matter

10. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yohsida (U. S. Patent No. 5, 036, 296) discloses sampling input signal with a signal having a phase different from the reference clock signal which is in synchronization with the input signal by a 1/2 clock cycle and then equalizing the sampled input signal.

Spurbeck et al. (U. S. Patent No. 6, 208, 481) discloses controlling the sampling using interpolation in a circuit including an adaptive equalizer.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 703-305-4097. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Curtis Odom
July 21, 2004

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600